REMARKS

The present Response is to the Office Action mailed 11/12/2008. Claims 17-22 and 31-36 are presented for examination.

Claim Rejections - 35 USC § 102

5.   Claims 17-19, 21, 31, 33, 34 and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by Malerevich et al (US 6,611,538).

Regarding claims 17, 18 and 31, Malerevich, as shown in figures 2-10, teaches apparatus and method for word synchronization between plurality of word devices (Fig. 4A-4C, A and B) in which the first device or second device requests synchronization between the two devices and data is being communicated upon synchronization between the two devices has been established. See also column 3, line 46 to column 5, line 49.

Regarding claim 19, Malerevich further teaches becoming unsynchronized in response receiving loss-of-synch signal. See column 7, line 46 to column 9, line 2.

Regarding claim 21, Malerevich further teaches resynchronizing after receiving bad control word. See column 7, line 46 to column 9, line 2.

Regarding claims 33 and 36, Malerevich further teaches entering loss-of synch state after receiving numbers of bad control word. See column 7, line 46 to column 9, line 2.

Regarding claim 34, Malerevich further teaches SERDES. See column 1, lines 21-52 and column 6, lines 1-9.

Claim Rejections - 35 USC § 103

8.   Claims 20, 22, 32 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malerevich et al (US 6,611,538).

Regarding claims 20 and 22, Malerevich teaches all subject matter claimed except for the loss-of-synch signal is being generated by the deserializer. See section 5 above. Instead, the loss-of-synch signal is being generated by the sync state machine (fig. 8, 106). However, it would have been obvious to one of ordinary skill in the art at the time

the invention was made to modify the invention of Malerevich by shifting the function of generating the loss-of-synch signal to the deserializer since it is just a matter of reassigning the function to a different element within the device.

Regarding claims 32 and 35, Malerevich teaches all subject matter claimed except for the threshold number of bad control words is one. See section 5 above. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Malerevich by entering unsynchronized state when only one bad control word is received since it is just a matter of setting the sensitivity of the device in response to the numbers of bad control word and such modification would not involve any inventive feature.

Applicant's response:

Applicant herein cancels claims 17-22 and 31-36 and provides new claims 42-44 for examination. Applicant's new claims more accurately reflect the subject matter sought for patent protection by applicant. Independent claim 42 provides a method for dividing the digital words into two or more word portions of equal bit length, the number of portions being an exponential power of 2. The art of Malerevich teaches data sent over a single serial line. Specifically, Malerevich teaches that synchronization is achieved using two bits per cell. The value of the two synchronization bits is changed on a cyclical basis for every cell. The two synchronization bits cycle through the values 00, 01, 10 and 11 cycling from one value to the next for every cell (col. 4, lines 47-54). Malerevich does not teach synchronization at word level over serial lines operating in parallel.

Applicant's claim 42 provides a step for transmitting each word portion from a serializer at one device to a deserializer at the other device on a separate serial line dedicated to each portion, the serial lines operating in parallel. This qualifies at least one 4 bit word divided into two 2 bit portions each simultaneously sent on a separate serial line to the same receiving device with the serial lines operating in parallel. Additionally the words could be 64 bits in a preferred embodiment, being divided into 8 bit word portions transmitted over 8 serial lines simultaneously.

Applicant points out that Malerevich teaches one serial link providing 52 bytes of data from one point to another (col. 3, line 64 to col. 4, line 6). Applicant's serializers also transmit, as a synchronizing sequence, an idle sequence including a first control word *simultaneously on each of the serial lines* to deserializers at the second device, which then enters a half-sync mode.

The Examiner states that Malerevich does not teach that the loss-of-synch signal is being generated by the deserializer. Instead, the loss-of-synch signal is being generated by the sync state machine (fig. 8, 106). However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Malerevich by shifting the function of generating the loss-of-synch signal to the deserializer since it is just a matter of reassigning the function to a different element within the device.

Applicant argues that there is a definite reason and value to transmitting each word portion from a serializer at one device to a deserializer at the other device, enabling synchronized receipt of the portions of digital words by the deserializers at the second digital device by transmitting by the serializers of the first device an enabling idle sequence including a first control word simultaneously on each of the serial lines, to the serializers at the second digital device, the second device then entering a half-sync mode, and eventually synchronizing, as claimed. Applicant points out that is the serializer/deserializer pairs that need to be synchronized to maintain word synchronization; and that this is fundamentally different than the synchronization taught in Melerivich.

Applicant's specification teaches that in order to accomplish word synchronization between devices 2 and 4, several operations must be carried out in a coordinated way as each word device operates as a transmitter or as a receiver for a 64-bit word. Acting as a transmitter, a device must send a data stream that enables the corresponding receiver to establish word synchronization. Acting as a receiver, a device must detect when word synchronization has been established or lost, notify a corresponding transmitter when there is no word synchronization, and request from a

corresponding transmitter that a sequence to enable word synchronization be sent. When a word device (e.g., device 2 or 4) is in the no-synch state, this indicates that the receiver at this end of the link does not have word synch. That is, the device is not prepared to synchronously receive 64-bit words. When a word device is in the half-sync state, this indicates that the device at this end of the link has word synch so that the device at the other end of the link may begin sending packets. However, there is no confirmation at the device at the other end of the link has word synch. A word output sequence is sent repeatedly as long as the device remains in the half- synch state. It enables the device at the other end of the link to become synchronized and notifies that device that this device has achieved word synchronization.

Malerevich teaches that sync state machine 106 comprises four states, Hunt 120, Pre Sync 122, Sync 124 and Lost Sync 126. The movement from one state to another is driven by the SYNC_FOUND and SYNC_NOT_FOUND signals generated by the count state machine. The sync state machine functions to control the mux selection input.

Applicant argues that it is the point of the present invention that the serializers and deserializers at each device keep each other in sync by directly communicating control words to each other. In this manner there is no reason to utilize a separate state machine. Therefore, it would not be obvious to do so.

Applicant believes the new claims 42-44 are patentable over the art of Malerevich as pointed out, above.

Summary

As all of the claims, as newly provided and argued above, have been shown to be patentable over the art presented by the Examiner, applicant respectfully requests reconsideration and the case be passed quickly to issue.

If any fees are due beyond fees paid with this amendment, authorization is made to deduct those fees from deposit account 50-0534. If any time extension is needed beyond any extension requested with this amendment, such extension is hereby requested.

Respectfully submitted
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